

MOTOROLA'S MC68302

INTEGRATED MULTI-PROTOCOL PROCESSOR

The MC68302 is a versatile one-chip processor that incorporates the main building blocks needed for the design of a wide variety of networking and communications products. The MC68302 was the first device to offer the benefits of a closely coupled, industry-standard, MC68000/MC68008 microprocessor core and a flexible communications architecture. This multi-channel communications device may be configured to support a number of popular industry-standard interfaces, including those for the Integrated Services Digital Network (ISDN) basic rate and terminal adapter applications. Through a combination of architectural and programmable features, concurrent operation of different protocols is easily achieved using the MC68302. Data concentrators, modems, line cards, bridges, and gateways are examples of other suitable applications for this versatile device. The MC68302 is an HCMOS device consisting of an MC68000/MC68008 microprocessor core, a system integration block (SIB), and a communications processor (CP).

Product Highlights

- MC68000/MC68008 Microprocessor Core
- Efficient architecture involves a separate RISC processor for handling communications
- Three Serial Communications Controllers (SCCs)
- Support for HDLC/SDLC, Bisync, UART, DDCMP, and Totally Transparent protocols.
- Two Serial Management Controllers (SMCs) for IDL and GCI Channel.
- Available at 16, 20, 25, and 33 MHz in three different Thin Quad Flat Pack Packages.
- Strong 3rd Party tools support.

MC68302 MICROPROCESSOR



Typical Applications

- ISDN equipment
- Data Concentrators
- Modems
- Line Cards
- Network Bridges
- Gateways

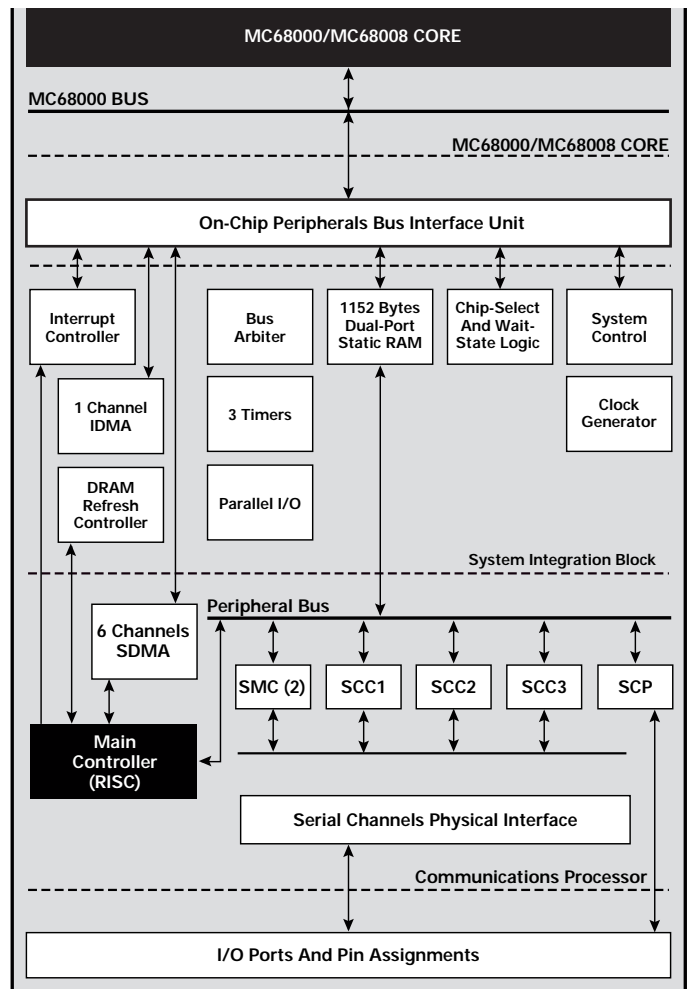
Technical Specifications

- MC68000/MC68008 Microprocessor Core
(May be disabled to use the IMP as a peripheral)

- Independent Direct Memory Access (IDMA) Controller
- Interrupt controller with two modes of operation
- Parallel I/O ports, some with interrupt capability
- On-Chip 1152-bytes of dual-port RAM
- Three timers, with a software watchdog timer
- Four programmable chip-select lines with wait-state logic
- Programmable address mapping of dual-port RAM and IMP registers
- On-Chip clock generator with an output clock signal
- System control
 - Bus arbitration logic with low interrupt latency support
 - System control register
 - Hardware watchdog for monitoring bus activity
 - Low power (Standby) modes
 - Disable CPU logic (M68000)
 - Freeze control for debugging selected on-chip peripherals
 - DRAM refresh controller

■ CP Including:

- Main controller (RISC Processor)
- Three full-duplex Serial Communication/Controllers with the following protocols:
 - HDLC/SDLC
 - Bisync
 - UART
 - DDCMP
 - Totally Transparent
 - V.110
- Six serial DMA channels dedicated to the three SOCs
- Capability to send/receive up to eight buffers/frames without M68000 core intervention
- Flexible physical interface accessible by SCCs for Inter-chip Digital Link (IDL), General Circuit Interface (GCI).
- Pulse Code Modulation (PCM), and Non-multiplexed Serial Interface (NMSI) Operation.
- Serial Communication Port (SCP) for synchronous communication.
- Two Serial Management Controllers (SMCs) for IDL and GCI Channel.



Contact Information

- Motorola offers user's manuals, application notes and sample code for all of its communications processors. In addition, local support for these products is also provided. This information can be found at:

<http://motorola.com/netcomm/>

- For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at:

Phone: 800-521-6274

MC68302 Derivatives

MC68LC302

- Static EC000 Core
- On-Chip PLL
- Low Power Modes Down in μ A Range
- Two SCC's
- 100-Pin TQFP

MC68EN302

- Full Ethernet 802.3 Compliant Controller Independent of SCCs
- Full DRAM Controller
- Parity Support
- Dynamic Bus Sizing
- Full Superset of 68302
- 144-Pin TQFP

MC68QH302

- 68000 Core Processor
- System Integration Block
- RISC Communications Processor
- Two SCCs
- One Dual Channel SCC
- Pin Compatible with 68302
- 144-Pin TQFP